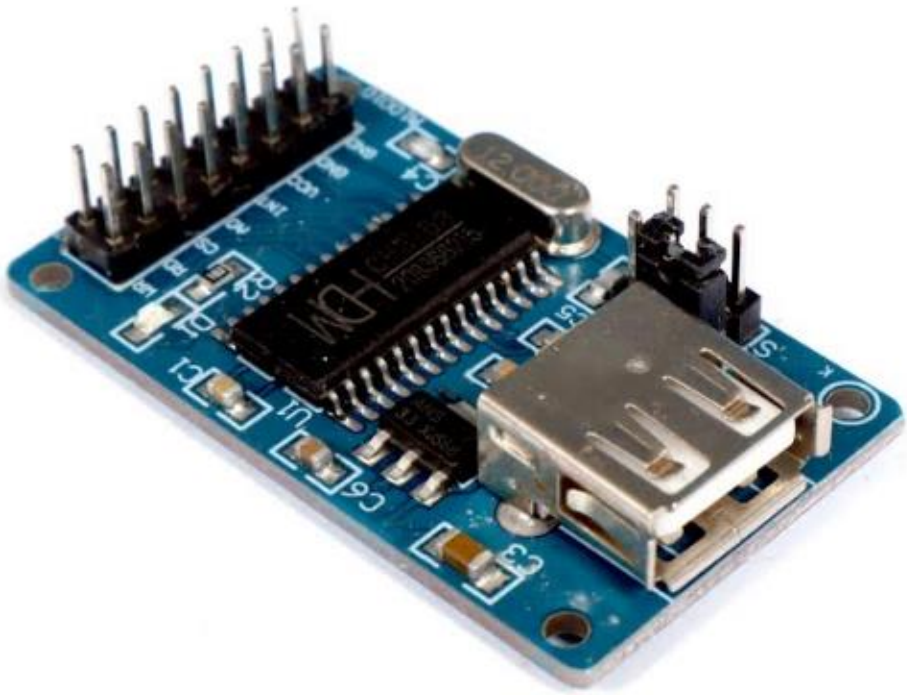
CH375B USB Disk Read- Write Module USB Flash Disk For Arduino



CH375 USB device mode is fully compatible with CH372, CH375 contains all the features of the CH372. Common CH375 USB host mode support USB full-speed device, the external microcontroller can through the CH375 in accordance with the USB protocol and USB device communication. CH375 firmware also built a dedicated protocol processing Mass-Storage mass storage devices, the external microcontroller can be directly used as the basic unit of reading and writing in sectors USB storage devices (including USB hard disk/USB flash drive/U disk).

CH375 with the 8-bit data bus and read, write, chip select control lines and interrupt output can be easily attached to the system bus of the microcontroller/DSP/MCU/MPU controller. USB host mode, CH375 also provides serial communication via serial input, serial output, and interrupt output monolithic/DSP/MCU/MPU connected.

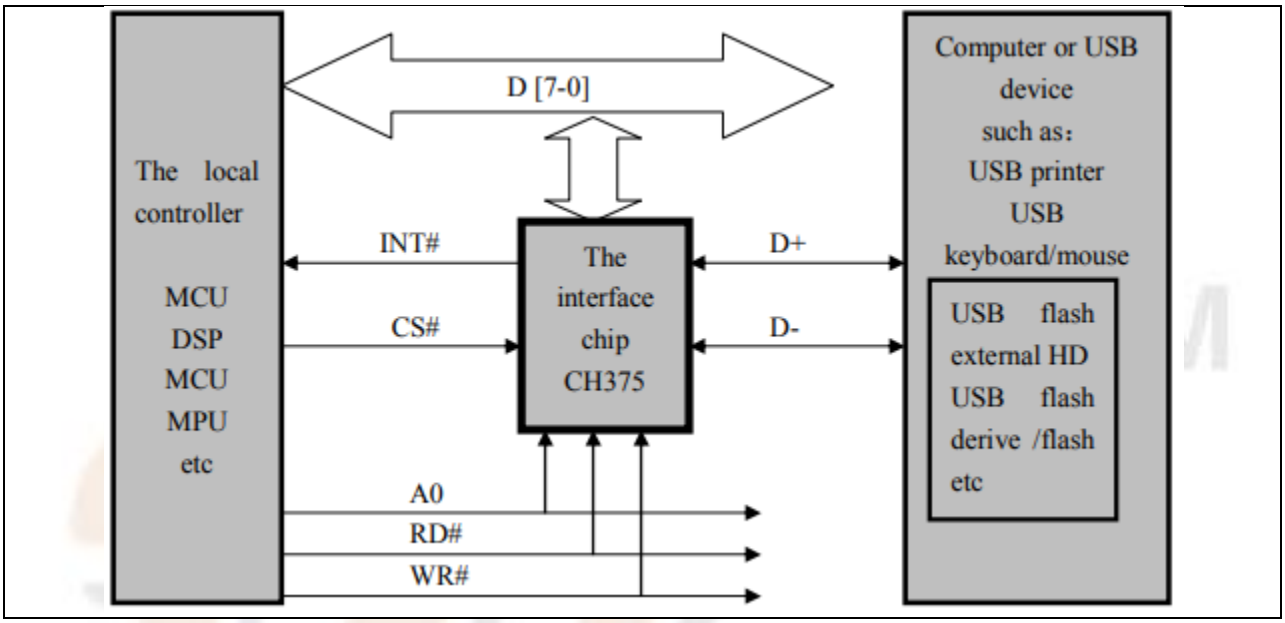
FEATURES:

- CH375B with the 8-bit data bus and read, write, chip select control lines and interrupt output can be easily attached to the system bus of the microcontroller/DSP/MCU/MPU controller.
- USB host mode, CH375B provides serial communication via serial input, serial output, and interrupt output monolithic/DSP/MCU/MPU connected.
- 2×8 connector, easy with the MCU mount.
- Jumper selectable can work in parallel or serial mode.
- USB status indicator.
- On board 3.3 V LDO 1117, provides 800 mA current.
- Colour: Blue

SPECIFICATIONS:

- IC Chip: CH375B
- LDO: 3.3V
- Input Voltage Range(VDC): 5
- Crystal: 12 MHz
- PCB Size (L x W) mm: 48 x 28
- Weight (gm): 6

FUNCTIONAL BLOCK DIAGRAM:



- CH375 is a USB bus universal interface chip, supports USB-HOST Mode and USB-DEVICE/SLAVE Mode. There are 8-bit data bus and read, write, chip select control wire and interrupt output in CH375.It is convenient to link CH375 to control system bus of MCU/DSP/MPU.CH375 also provides serial communication in USB-HOST mode. It connects with DSP/MCU/MPU through serial input, output and interrupt output.
- The USB device mode of CH375 is compatible with CH372, and CH375 incorporates all functions of CH372. For USB-DEVICE/SLAVE mode operation and specification, please refer to the CH372 specification. This data sheet only covers USB-HOST mode operation. The USB-HOST mode of CH375 supports common USB full-speed devices. Peripheral MCU can communicate with USB device through CH375 according relevant USB protocol.
- The CH375 configures firmware of special communication protocol inside which can deal with Mass-Storage. Peripheral MCU can read and write general USB store devices (including USB HD, USB flash and USB flash drive) directly while sector as unit.

Location hardware:

- The CH375 gives common passive parallel and point-to-point serial interface in location. During the reset time of CCH375, pin TXD is used to choose communication interface. If CH375 check TXD as low-level during reset time, then start parallel interface, otherwise start serial interface. If starting serial interface, the TXD pin is used to serial data output after reset, and CH375 can only work on the USB host mode.

Parallel interface:

- The parallel interface signal wires contain 8-bit bi-directional data bus D7 to D0, read selection input pin RD#, write selection input pin WR#, chip selection input pin CS#, interrupt output pin INT# and address input pin A0.The CH375 is easily attached to system bus of multifarious MCU with 8-bit, DSP and MCU through passive parallel interface. Also coexist with many peripheral parts.
- The CS# of CH375 is driven by address decoding circuit used to select device while MCU embody many peripheral equipments.
- The output of interrupter request with INT# is valid when it is low-level and connects to interrupter input pin or common I/O pin of MCU. The MCU may get the interruption through interrupter manner or detection manner. For parallel time schedule MCU similar with Intel, the RD# and WR# of CH375 can separately connect with read strobe output pin and write strobe output pin.
- For parallel time schedule MCU similar with Motorola, the RD# of CH375 must connect with low-level, and WR# connect with R/-W of MCU. CH375 occupies two address bits. When A0 is high-level, choose command port, write new command or read interrupt token; when A0 is low-level, choose data port, read and write data. The following table is operation value table of parallel interface I/O (in the table X show that don't care the bit, Z show that the tri-state is forbidden of CH375).

CS#	WR#	RD#	A0	D7-D0	Operation for CH375
1	X	X	X	X/Z	Don't choose CH375, no operation
0	1	1	X	X/Z	Choose CH375, but no operation
0	0	1/X	1	IN	Write command code to CH375's command port

0	0	1/X	1	IN	Write data to CH375's data por
0	1	0	0	OUT	Read data from CH375's data port
0	1	0	1	OUT	Read interrupt token from CH375B's command port, the bit 7 is equal to INT#

Serial interface:

- Serial interface is only used to USB-HOST mode while USB-DEVICE/SLAVE is unsupported. The serial interface signal wires contain serial data input pin RXD, serial data output pin TXD and interrupt output pin INT#. The CH375 connects of MCU, DSP and MCU point-to-point for a distance using the least connections through the serial interface.
- The RXD and TXD of CH375 can connect to the serial data output pin and serial data input pin of MCU respectively. The output interrupter request of INT# is low-level valid to inform to MCU. Format of CH375's serial data is composed of one starting bit、nine data bits and one stopping bit while the former eight data bits are one byte, the later is command flag bit.
- The former eight data are written to CH375 while the 9 bit is zero. The former eight data are written to CH375 as command code when the ninth is logical 1.The serial communication baud rate is 9600bps in default as MCU can select appropriate communication baud rate at any time through command SET_BAUDRATE.

Other:

- The ACT# shows state in CH375.The pin output high-level while device is not configured or cancel configuring of USB in the mode of USB-DEVICE setting firmware internal. The pin outputs low level after configure USB device. In the USB-HOST mode, ACT# outputs high-level when USB device detach in USB-HOST mode. The pin will output low-level after USB device connection. The ACT# pin of CH375 can attach to current-limited resistance LED to indicate relative state.
- UD+ and UD- are signal bus of USB directly connect to USB bus when works in the USB-DEVICE mode. They can attach to USB device directly on USB-HOST. The direct

or alternating current equal serial resistance is within 5Ω which protects chip to serial link of insure resistance, inductance or ESD.

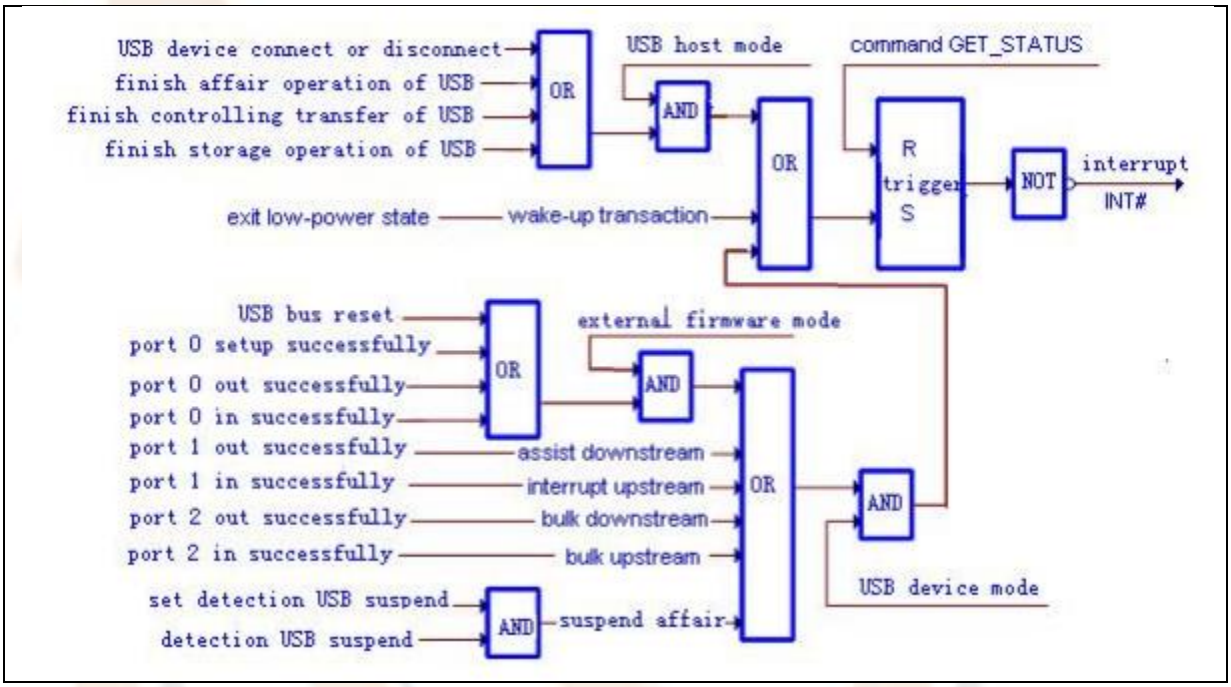
- The chip CH375 set power-up reset circuit inside, and external supplies reset is not need in generally. RSTI inputs asynchronous reset signal from outside. The ch375 is reset when RSTI is high-level. When RSTI recovered to low-level, CH375 will go on time-lapse reset about 20mS and step into work normally. In order to reduce external disturb and make sure of reset during power-up, capacitance about 0.47uF can attach between RSTI and VCC. RST and RST# are output reset state pin, act with high-level and low-level respectively.
- They output high-level and low-level respectively if CH375 is power-up reset or forced to reset by outside circuit or reset time-lapse. After reset RST and RST# recovered to low-level and high-level. RST and RST# offer power-up reset signal to external MCU. The CH375 needs outside clock of 12MHz to work normally. In common, clock signal is generated by inverter in CH375 through oscillating of crystal keeping frequency. A crystal of 12MHz between XI and XO, XI and XO connect a high frequency oscillator capacitance to ground respectively can compose the peripheral circuit. The 12MHz clock signal directly input to XI while suspending XO. CH375B supports 3.3V or 5V .
- The VCC pin inputs external 5V power and V3 pin connects to power decoupling capacitance with the capacity from 4700pF to 0.02uF when with 5V power. The V3 must attach to VCC and input external 3.3V power while work power is 3.3V.In addition, the power of other circuit connection of CH375 is not surpass 3.3V.

Internal configuration:

- In the inner of CH375 integrate PLL multiplier, the host and slave USB interface SIE, data buffer, passive parallel interface, asynchronous serial interface, command explanation device, protocol transaction device to control transmission, firmware program in common etc.
- PLL multiplier takes the 12MHz input from clock and generates a 48MHz reference clock for SIE. Host-slave USB interface SIE mixes the USB-HOST mode with USB-DEVICE mode.

- It takes charge of physical USB data receive and transfer, deals with bit track and synchronization automatically, coding and decoding of NRZI, bit stuffing, parallel/serial data conversion, CRC data check, transaction handshake, retry when error, detection USB bus state etc.
- Data buffer delays data receive and transfer of USB interface SIE. Passive parallel interface exchanges data with peripheral MCU/DSP/MUC. Asynchronous serial interface exchanges data with peripheral MCU/DSP/MUC substance of passive parallel interface. Command explanation device analyzes and executes various commands from peripheral MCU/DSP/MCU.
- Protocol transaction device deals controlling transfer at many layers automatically to simplify peripheral firmware program.
- Common firmware program contains two groups. One group used to USB-DEVICE to treat with numbers of normal affairs in default port 0 of USB automatically.
- The other used to USB-HOST, handles with special communication protocol in Mass-Storage automatically. There are seven endpoints in CH375 inner. The port0 is a default endpoint, supports up streaming and down streaming.
- The buffer of upstream and downstream is 8-byte respectively. The port1 includes upstream and downstream endpoint and buffer of each is 8-byte. The upstream endpoint number is 81H while the downstream endpoint number is 01H. The port2 includes upstream and downstream endpoint and buffer of each is 64-byte. The upstream endpoint number is 82H while the downstream endpoint number is 02H.
- The host endpoints include output and input endpoint, and each buffer is 64 bytes. The host endpoint is operable to port2 with one buffer. T
- he output buffer of host is the upstream buffer of port2 as the input buffer of host is downstream buffer of port2. The port0, port1 and port2 of CH375 are used to USB-DEVICE mode while the host endpoint is used to USB-HOST. The CH375 supports various common USB full-speed devices in the USB-HOST mode.
- The endpoint number of USB device varies from 0 to 15 and the two directions can support 31 ports at best.
- The package length of USB device varies from 0 to 64 bytes. The peripheral firmware deals with communication protocol of Mass-Storage device and commands USB storage

device to satisfy the following requests: supports Bulk-Only transfer protocol , supports SCSI, UFI, RBC and other equivalent storage device which accommodates the minimum set of command, the longest package length of data endpoint is 64-byte but the longest package length of default endpoint is 8, 16, 32 or 64 bytes. If the USB storage device isn't according to requests, the peripheral MCU must deal with referred communication protocol automatically through control transfer and ISSUE_TOKEN command or ISSUE_TKN_X. The following is interrupt logical drawing inner of CH375.



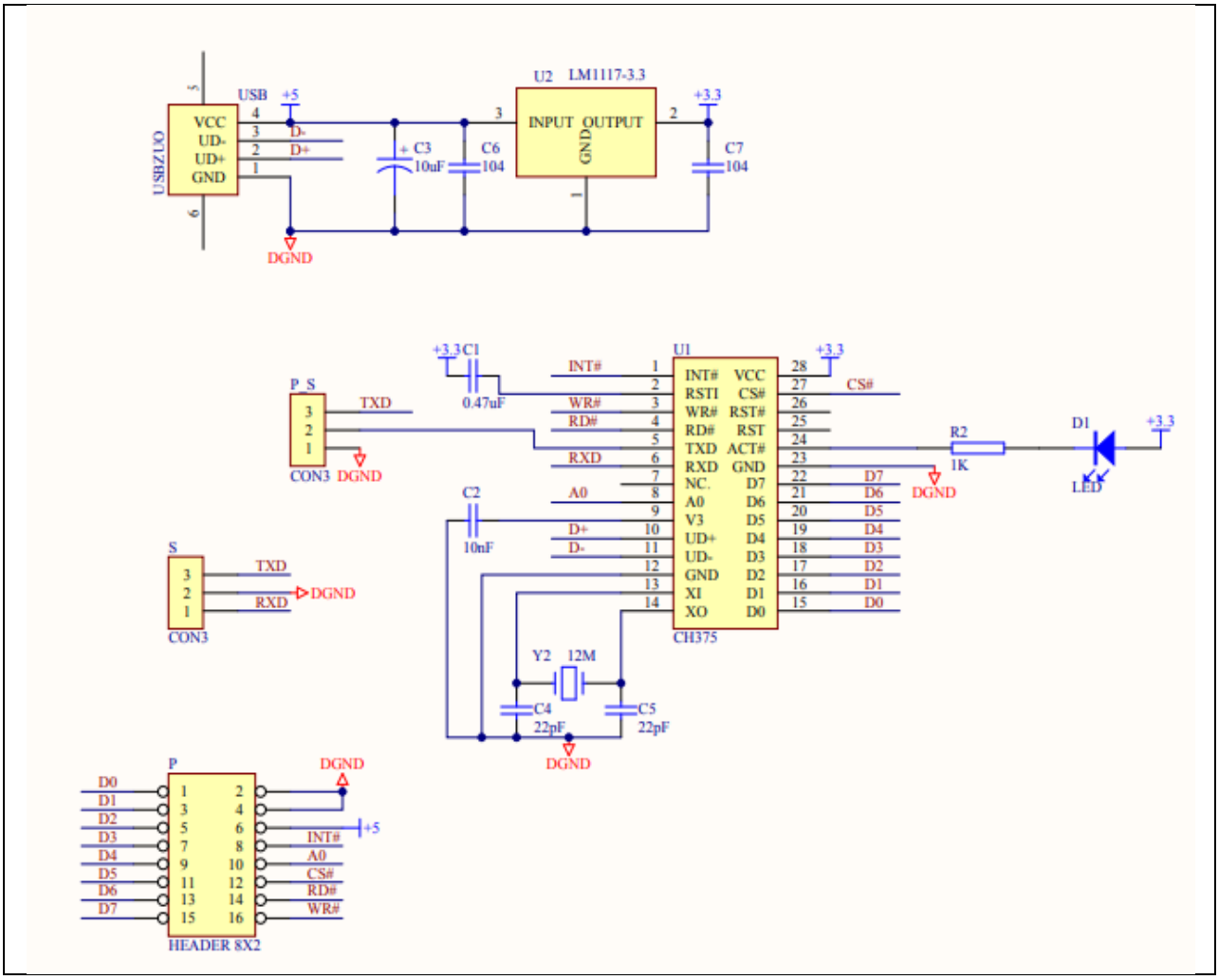
Local MCU software:

- MCU read from or write to CH375 through 8-bit parallel interfaces. Each operation is composed of one command, several input data and several output data. Some commands don't need input data while some command don't have output data. The following is command operation process:

1. Write command code to command port while A0=1.
2. If the command has input data, then write input data one byte each time when A0=0.
3. If the command has output data, then read output data one byte each time when A0=0.

4. After the command is finished , pause or return to ① to execute next command. The CH375 is specially handling USB communication. It will inform the MCU to deal with through interrupt manner when detection the change of USB bus or command is finished.

SCHEMATIC DIAGRAM:



PIN FUNCTION:

Pin No	Pin Name	Pin Type	Pin Description
28	VCC	POWER	Positive power input port, requires an external 0.1uF power decoupling capacitance
12, 23	GND	POWER	Public ground, ground connection for USB
9	V3	POWER	Attachment of VCC input external power while 3.3V;connects of 0.01uF decoupling capacitance outside while 5V
13	XI	IN	Input of crystal oscillator, attachment of crystal and crystal oscillator capacitance outside
14	XO	OUT	Opposite output of crystal oscillator, attachment of crystal and crystal oscillator capacitance outside
10	UD+	USB signal	USB Data Signal plus
11	UD-	USB signal	USB Data Signal minus
22～15	D7～D0	Bi-directional tri-state	8-bit bi-directional data bus, with pull-up resistor
4	RD#	IN	Read Strobe Input, an active LOW input, with feeble pull-up resistor
3	WR#	IN	Write Strobe Input, an active LOW input, with feeble pull-up resistor
27	CS#	IN	Active LOW CH375 chip select, With feeble pull-up resistor
1	INT#	OUT	Interrupter request output after reset, active with low-level
8	AO	IN	Address wire input to identify command and data port, with feeble pull-up resistance, A0=1,write order; A0=0,read/write data
24	ACT#	OUT	After USB device configure output state on firmware Inside USB-DEVICE mode, active with low-level under USB-DEVICE; USB device connection state output under USB-HOST, active with low-level
5	TXD	IN OUT	Used to USB-HOST only, supports parallel interface in USB-DEVICE, input pin, with feeble pull-up resistor, enable parallel interface otherwise serial interface during reset input low-level, after reset is serial data output
6	RXD	IN	Serial data input, with feeble pull-up resistor
2	RSTI	IN	Reset input external, active with high level, with pull-down resistor
25	RST	OUT	Reset with power-up and external reset output,

			active with high-level
26	RST#	OUT	Reset with power-up and external reset output, active with low-level
7	NC	NC	Must be left unconnected

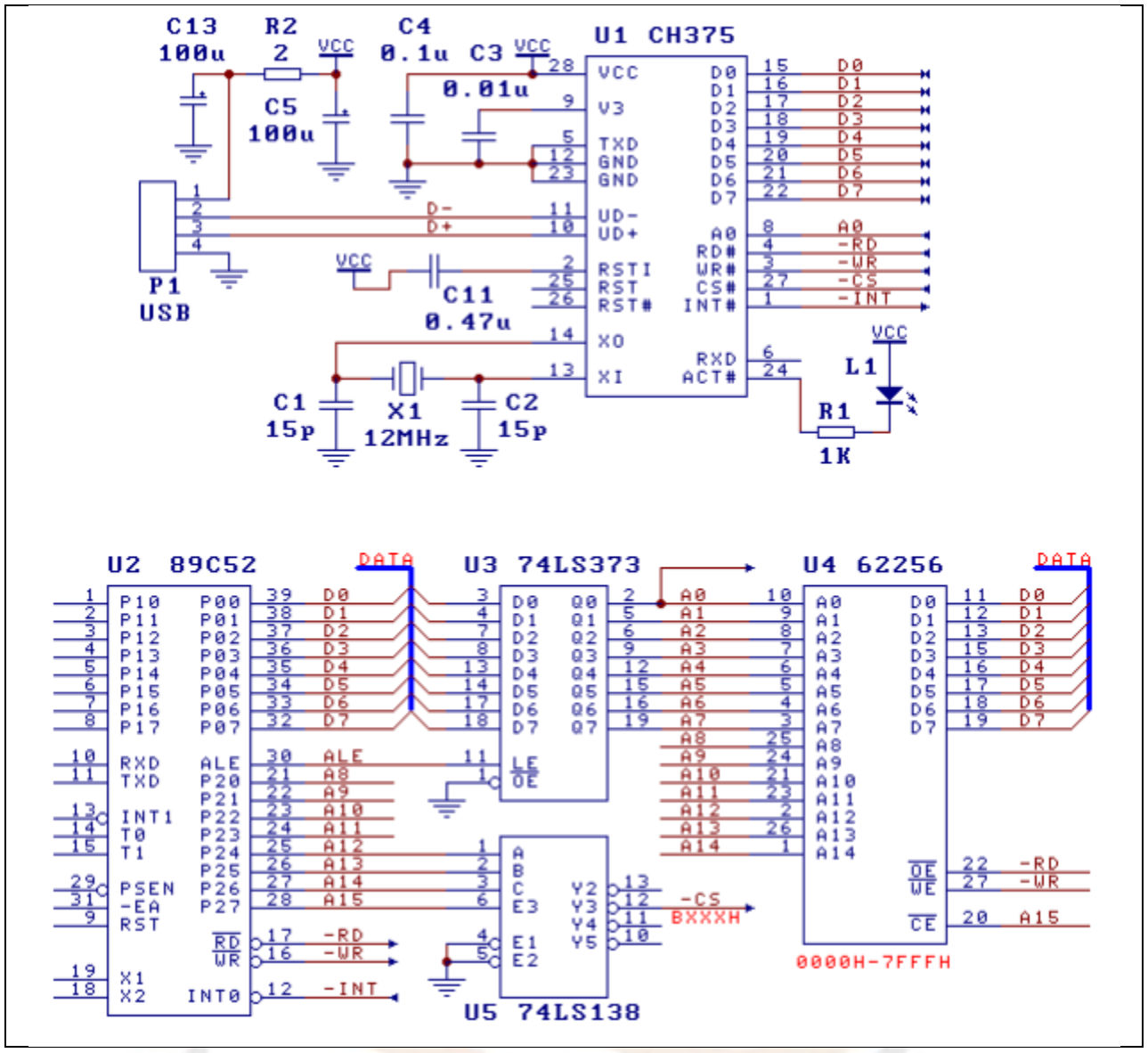
APPLICATIONS:

- Wide consumer products
- Water proofed electric products
- Button key replacement

TYPICAL APPLICATION CIRCUIT:

Parallel interface mode:

- The following diagram is CH375 connection of common MCS-51 circuit. The TXD of CH375 connects to ground through about 1KΩ pull-down resister or directly connects to ground. So the CH375 works on the parallel manner.



- The USB bus contains a double power bus and a double data signal bus. Usually, +5V power wire is red, ground wire is black, D+ signal wire is green and D- is white. The USB receptacle P1 connects to USB device directly. In need, serial connects flash switch with limiting current in +5V power bus that supplies to USB device. The USB power must be 5V. The capacitance C3 eliminates the coupling of inner power of CH375.The capacity of C3 is 4700pF to 0.02uF.It is made of monolithic or high frequency ceramic.
- The C4 and C5 are used to decoupling of external power. The C4 is 0.1uF and made of monolithic or high frequency ceramic. The crystal X1, capacitance C1 and C2 are

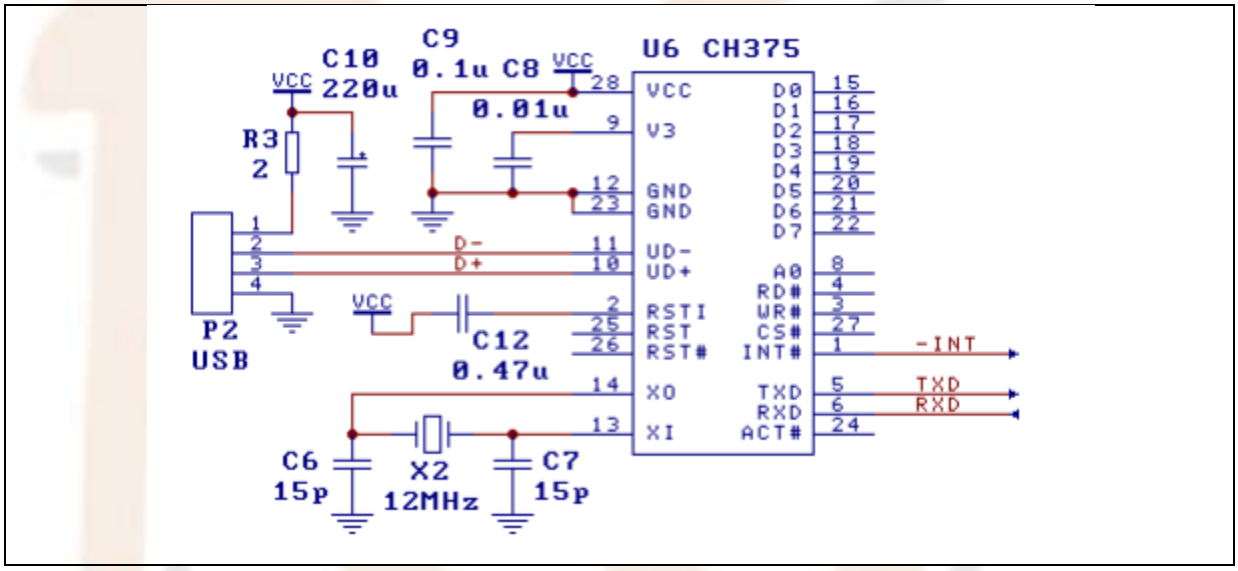
composed of clock oscillating circuit of CH375.The USB-HOST mode needs exact frequency.

- The frequency of X1 is 12MHz±0.4‰,C1 and C2 are monolithic or high frequency ceramic capacitors of 15pF～30pF. In order to reset CH375 credibly, the time is below 100mS when the power raises from 0V to 5V.If the process of power-up is slow and discharge is not in time when cut the power, and the CH375 reset is not credible. One solution is to connect a capacitance of 0.47uF between RSTI and VCC to delay the reset time.
- If the source power of CH375 is 3.3V, connect V3 and VCC, and input 3.3V, take the C3 out. When designing the PCB, pay much attention to some notes: decoupling capacitance C3 and C4 must keep near to connection pin of CH375; makes sure D+ and D- are parallel and supply ground net or pour copper beside them to decrease the disturbance from outside signal; the relevant signal between X1 and X2 must be kept as short as possible. In order to lessen the high frequency clock disturbance, play ground net or pour copper to the relative equipment.
- The CH375 has the common passive parallel interface, connects to various MCU, DSP and MCU directly. In common MCS-51 typical application circuit, CH375 can connects to system bus of MCU through 8-bit passive parallel interfaces D7～D0, -RD, -WR, -CS and A0. If the MCS-51 has not lock A7 ～A0 through U3,uses the P20 of U2 to drive the address bus A0 of CH375 and modify the port address of MCU program.U4 takes charge of simple address encoding, produces chip selection signal in need.
- The chip selection address varies from B000H to BFFFH of CH375 in the image while occupies two address in actually. The BXX1H used to write commend as the BXX0H used to read or write data.

Serial interface mode:

- The CH375 works in serial interface mode while the TXD is suspended or connection of ground without pull-down resistance.
- In the mode, CH375 only to connect to MCU/DSP/MCU through three signal pin such as TXD,RXD and INT#, others may suspend.

- The peripheral circuit is the same to the parallel mode except fewer connection pin. In addition, mends communication baud-rate dynamically, one suggest is that controlling RSTI of CH375 through MCU I/O point in order to reset CH375 to default baud-rate.
- Driving the RSTI through the standard bi-direction I/O point of MCS51 may add several KΩ pull-up resistors because of RSTI setting inside of pull-down resistance. Because of the INT# and TXD only supply faint high-level output current during reseting, on the further distance connection, in order to avoid disturb INT# or TXD during reset of CH375,one 2KΩ to 5KΩ pull-up resistance can add to INT# or TXD to keep the high-level steady. After reset, the INT# and TXD may enable to supply 5mA high–level output current or 5mA low-level draft current.



PACKAGE INCLUDES:

1 x CH375B USB Disk Read-write Module USB Flash Disk For Arduino